NONVOLATILE SEMICONDUCTOR MEMORIES

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MOUNTAIN VIEW, CA. 94043

11 MAY, 1984

NONVOLATILE SEMICONDUCTOR MEMORIES

- CLASSIFICATION BY FUNCTION
  - ROM
  - PROM
  - EPROM
  - E^2PROM
- CLASSIFICATION BY TECHNOLOGY
  - INTERCONNECT DEPENDENT STORAGE
  - FLOATING GATE STORAGE
  - GATE INSULATOR STORAGE

The greatest-capacity nonvolatile memories available commercially.

Type	Capacity	Bits per chip	Cost, $	Cost per bit, $	Technology	Line width, µm	Average access time, ns	Power dissipation, mW	Manufacturer
ROM	1 mb	1 048 576	—	—	CMOS	2.0	350	70	Hitachi Ltd.
PROM	64 kb	65 536	50	0.000763	Bipolar	4.0	40	120	Fairchild Camera and Instrument Corp.
	64 kb	65 536	50	0.000763	Bipolar	4.0	40	770	Fujitsu Ltd.
	64 kb	65 536	100	0.001526	Bipolar	5.0	60	900	Harris Corp.
EPROM	256 kb	262 144	87	0.000332	NMOS	2.0	200	550	Intel Corp.
	256 kb	262 144	334	0.001274	NMOS	2.5	170	525	Advanced Micro Devices
E²PROM	64 kb	65 536	—	—	MNOS*	2.1	200	825	Inmos Corp.

Mark A. Fischetti

IEEE spectrum JANUARY 1984

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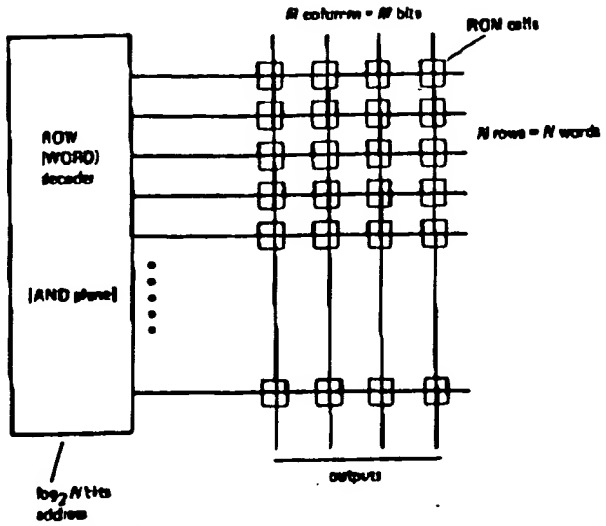
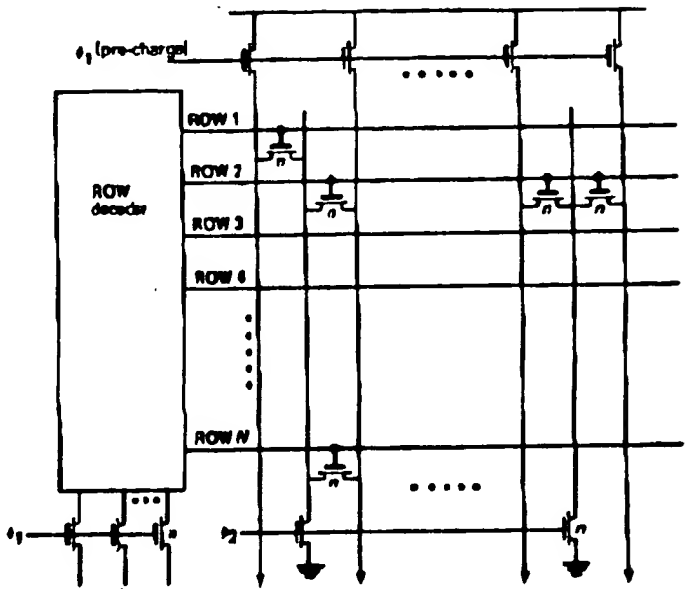


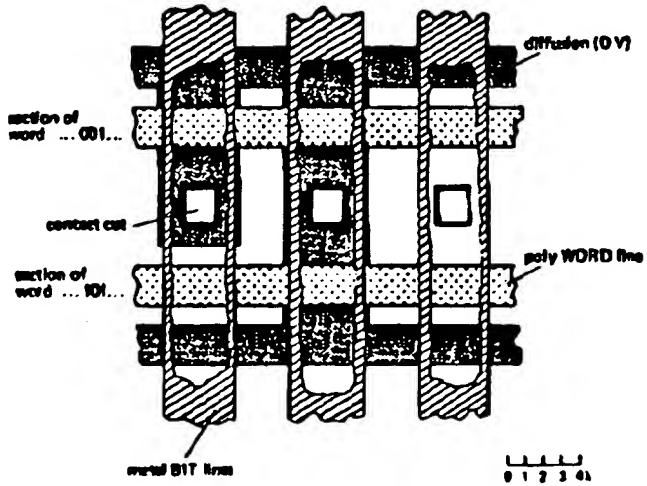
Basic ROM configuration.



Dynamic ROM arrangement.

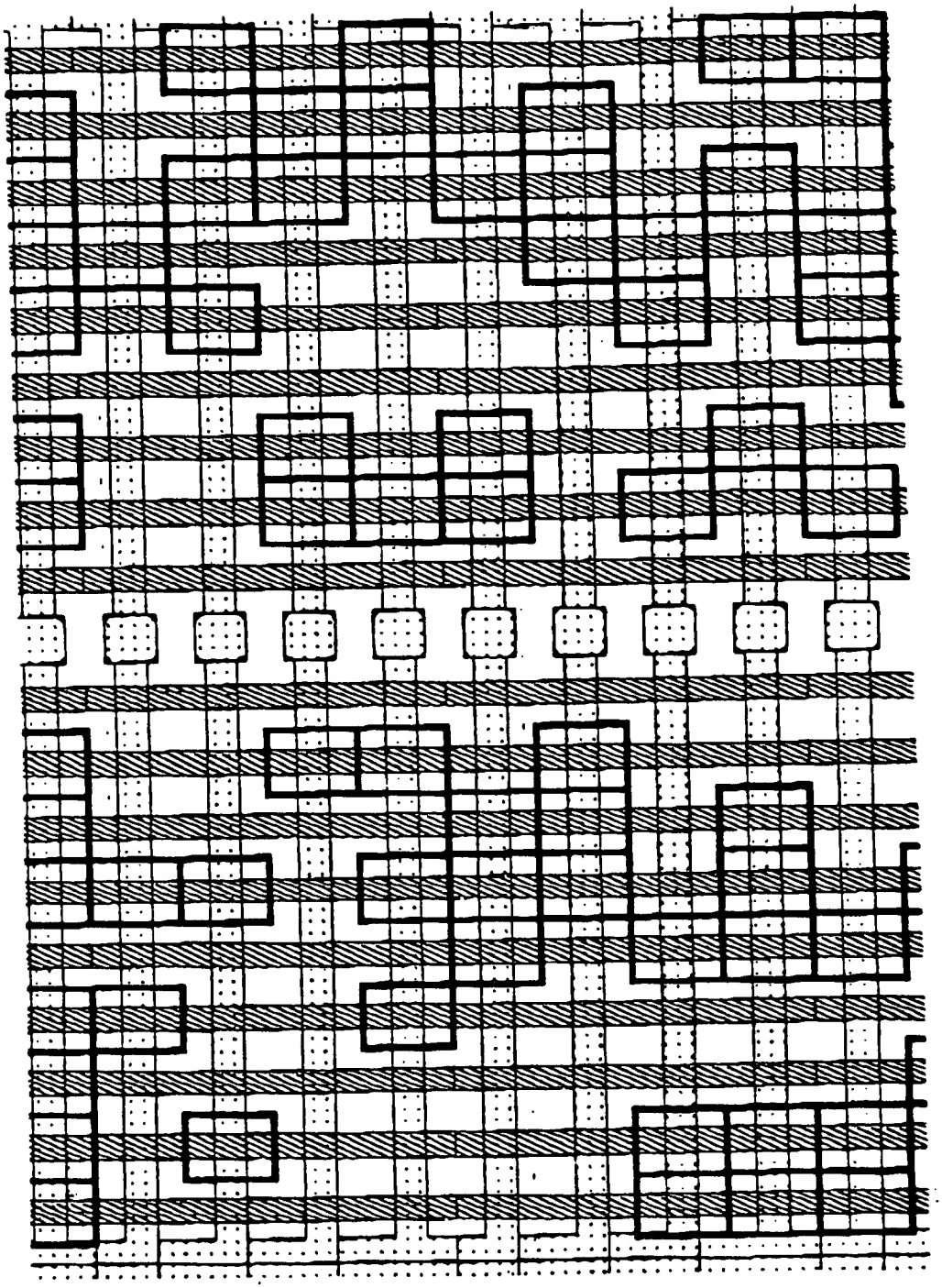
Introduction to MOS LSI design

J. MAVOR, M. A. JACK, P. B. DENYER



Simple ROM cell (silicon-gate NMOS) with metal bit lines shown cut away to reveal programming transistors.

DEPLETION MASK PROGRAMMING OF MOS ROM



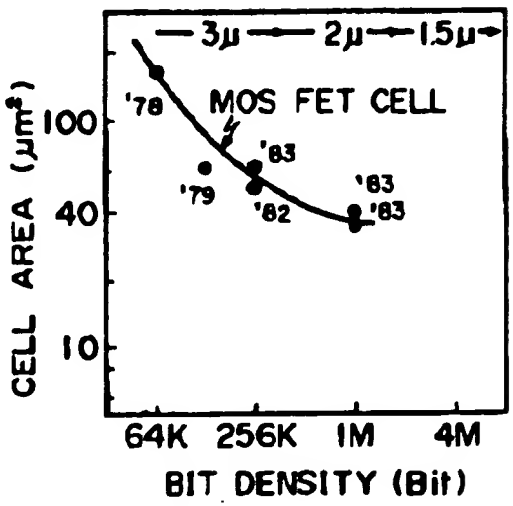
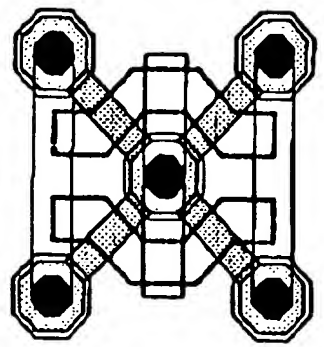


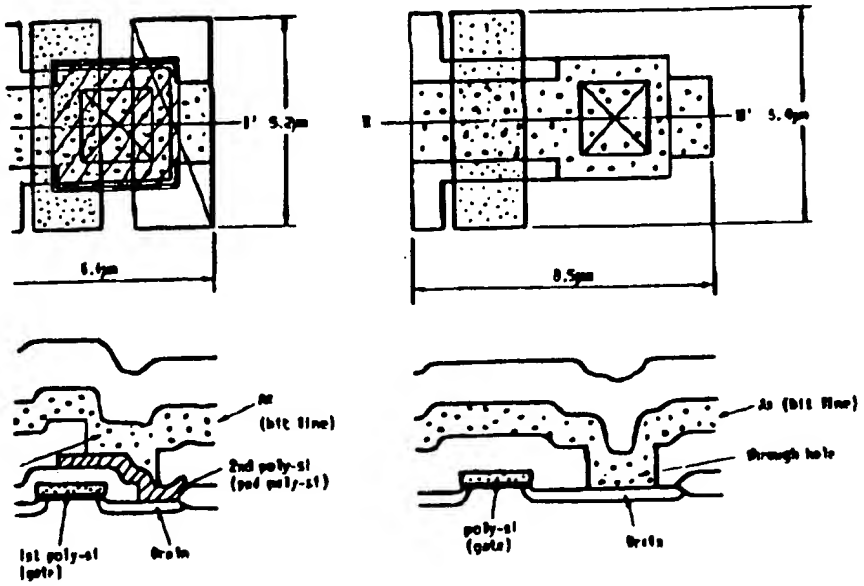
Fig.1. Cell area versus bit density for mask ROMs in the past 5 years.



An 80ns 1Mb ROM

Fujio Masuoka, Shoji Arizumi, Taira Iwase, Michihiro Ono, Norio Endo

Toshiba Corp.



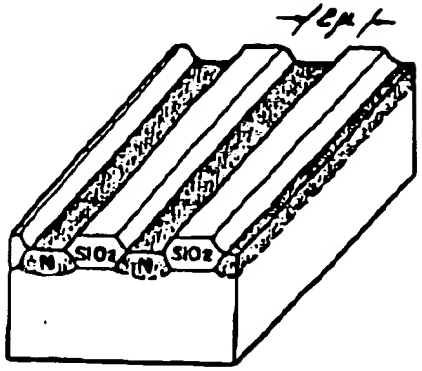
(a) New cell (b) Current cell

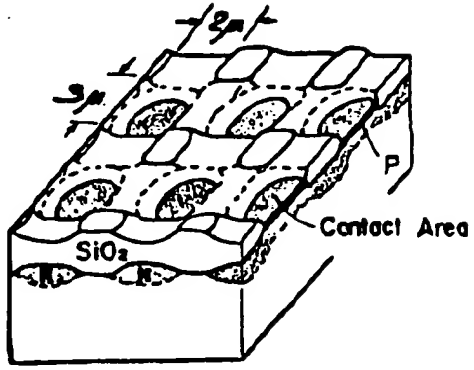
		Current structure		New structure
		Programming by field oxide or channel ion implantation	Programming by through hole	Programming by through hole
Programming process	Present flow			
	1. Field oxide growth	prog. field oxide		
	2. Gate oxide growth			
	3. Channel implant	prog. channel implant		
	4. Poly-Si deposition			
	5. Source and drain diffusion			
	6. Passivation			
	7. Contact hole etching		prog. through hole	prog. through hole
	8. Al metallization			
cell size (μm^2) (2.0μm ground rule)		5.0 × 9.7	5.0 × 8.5	7.1 × 8.4
1M bit chip size (mm^2)		80.4	72.2	91.5
turn around time		long ×	short ○	short ○
chip size		small ○	large ×	small ○
structure		single poly-Si	single poly-Si	double poly-Si

TABLE 1—Comparison of characteristics of new structure and current structure.

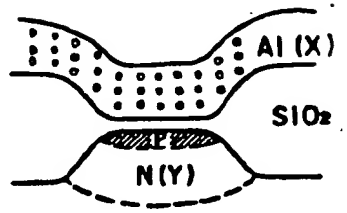
Technology	P-well CMOS Double Poly-Si gate Fully static sense amp with negative feedback
Organization	128K words × 8b
Cell size	5.2 × 6.4μm^2
Chip area	7.08 × 7.7mm^2
Address access time	80ns
Cycle time	80ns
Power supply	5V
Active current	8mA at 200ns cycle time
Standby current	0.01μA
Package	28 pin, 600 mil DIP

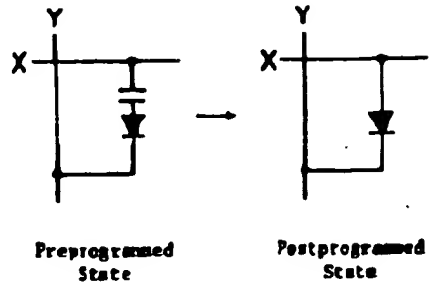
TABLE 2—Summary of typical characteristics.





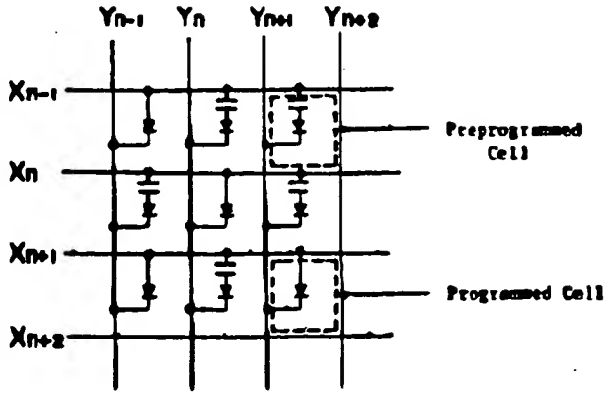
The Double LOCOS (DL) process.





(a) (b)

(a) The cross section of the SADL cell structure. The cell consists of a pn-diode contact area covered by a thin SiO_2 layer. (b) The equivalent circuit of the cell.



An example of the programmed SADL cell array.

IEDM 83

A NEW CELL FOR HIGH CAPACITY MASK ROM BY THE DOUBLE LOCOS TECHNIQUE

Noriaki Sato, Takahiro Nawata, and Kunihiko Wada

IC Development Division, Fujitsu Limited

CMOS PROM with Polysilicon Fusible Links

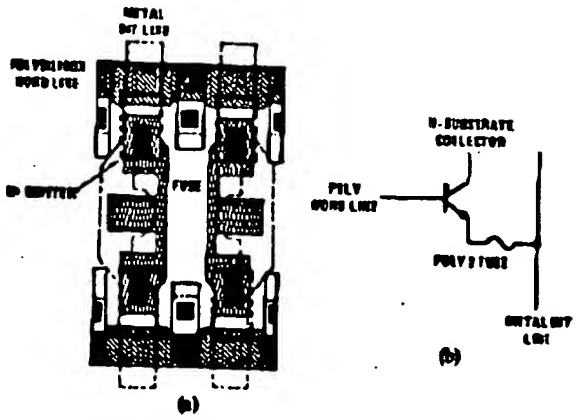


Fig. 1. (a) Layout of the 4-bit cell. (b) Single-bit equivalent circuit.

Fig. 2. SEM photograph of a 4-bit cell.

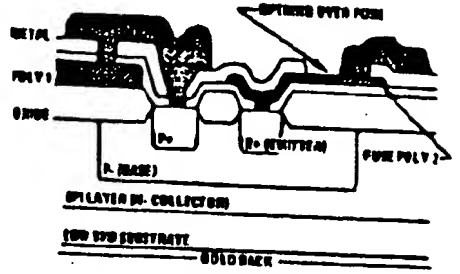


Fig. 3. Profile of the process.

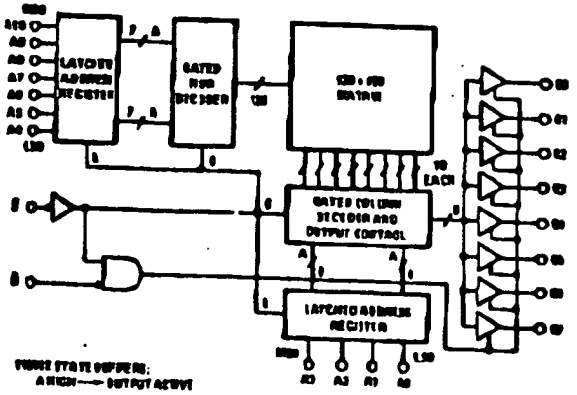
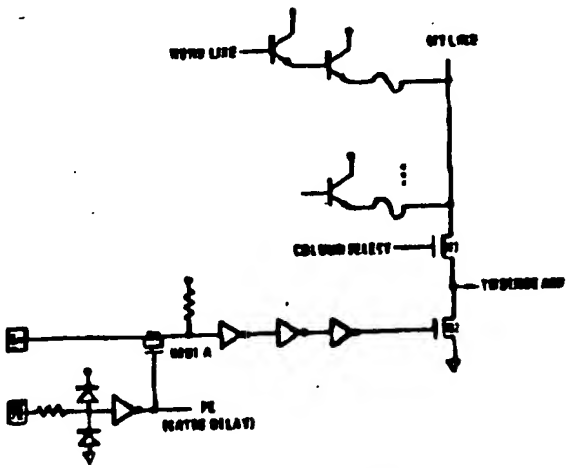
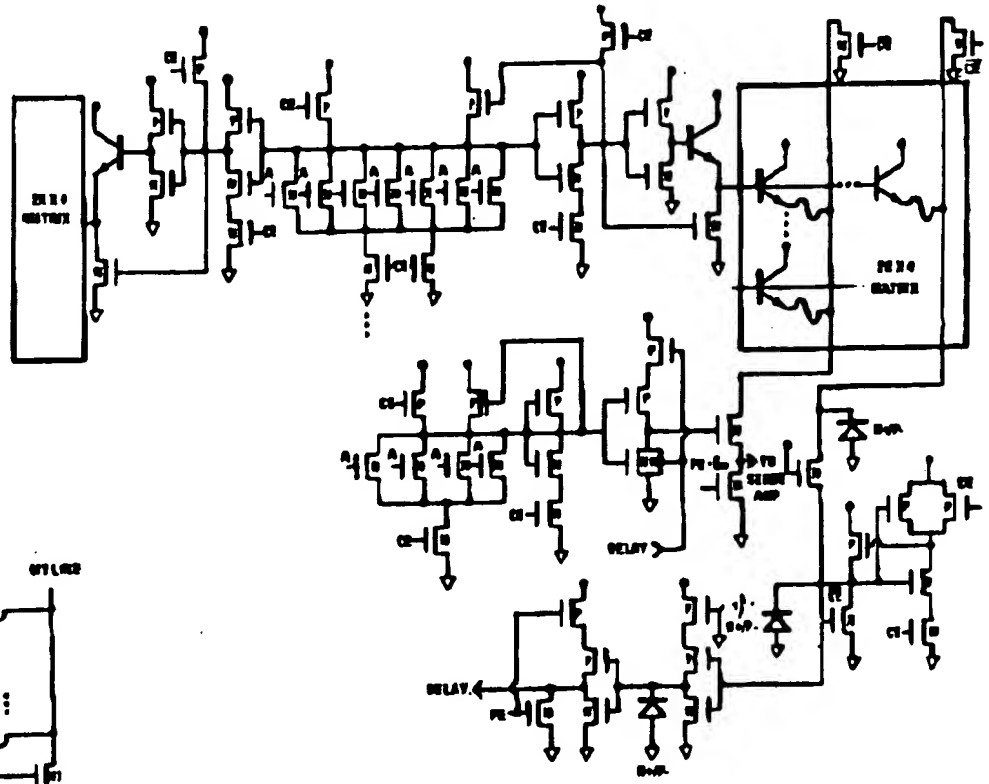


Fig. 4. Block diagram of the PROM.



The programming circuitry.



Schematic of read path and delay circuit.

TABLE I
TYPICAL DEVICE CHARACTERISTICS

ORGANIZATION	1K WORD × 8 BIT
DIE SIZE	3.88 × 5.8mm
CHANNEL LENGTHS	
N-CHANNEL	2.0μm
P-CHANNEL	2.0μm
GATE OXIDE	450Å
JUNCTION DEPTH	
N+	0.2μm
P+	0.3μm
THRESHOLDS	
N-CHANNEL	.75V
P-CHANNEL	.75V
CHIP ENABLE ACCESS TIME	70nsec
STANDBY POWER DISSIPATION	6μW
ACTIVE POWER DISSIPATION	10mA/MHZ

Junction-Shorting PROM

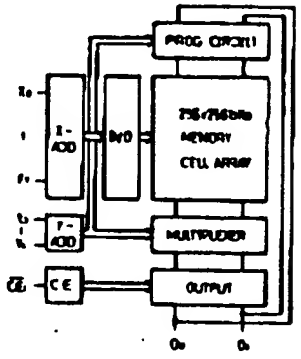


Fig. 1. Block diagram of a 64 kbit PROM with an 8192 word×8 bit organization.

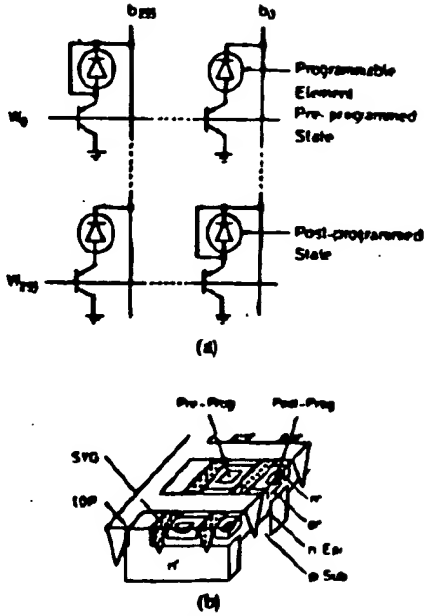
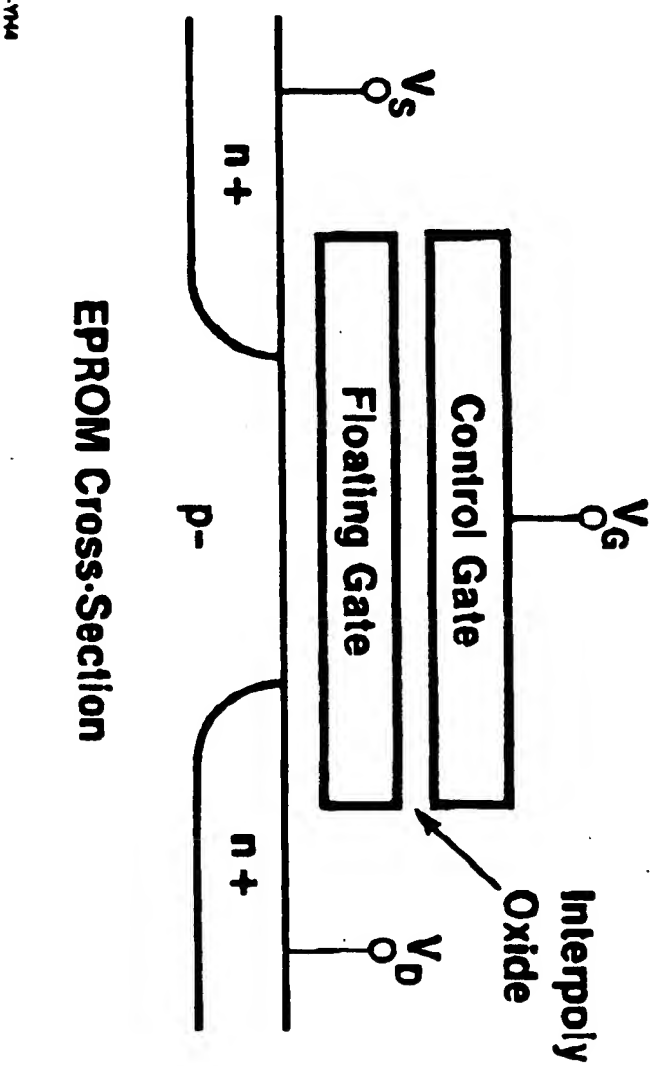
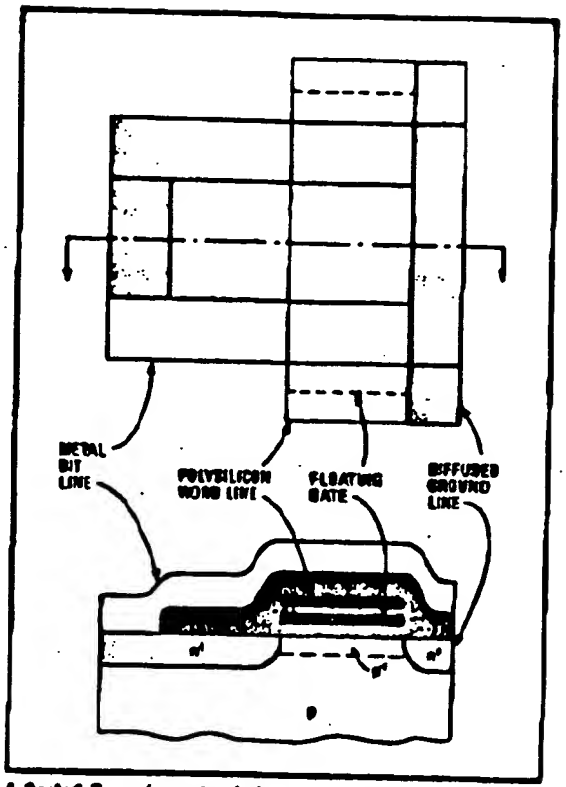


Fig. 2. Partial equivalent circuit and cross section of memory cell array. (a) Combinations of programmable element (p-n diode) and p-n-p transistor. (b) Cross section.

SCALING DATA FOR THE 256-K ERASABLE PROGRAMMABLE READ ONLY MEMORY					
Parameter	64-K chip	Constant field scaling formula	Theoretical 256-K chip	Actual scaling formula	Actual 256-K chip
Cell area	180 μm²	K^{-2}	40 μm²	$\approx K^{-2}$	36 μm²
Floating-gate oxide	725 Å	K^{-1}	380 Å	$\approx K^{-1}$	326 Å
Control-gate oxide	800 Å	K^{-1}	450 Å	K^{-1}	450 Å
Channel doping	9 x 10¹⁶ cm⁻³	K	6 x 10¹⁶ cm⁻³	[illegible]	6 x 10¹⁶ cm⁻³
Threshold voltage	[illegible] V	K^{-1}	0.8 V	1	[illegible] V
Cell current	56 μA	[illegible]	30 μA	[illegible]	80 μA
Read voltage	5 V	[illegible]	2.8 V	[illegible]	[illegible] V
Program voltage	21 V	K^{-1}	11 V	$K^{-0.7}$	13 V

Electronics/February 24, 1983


1384-YH4
EPROM Cross-Section
V_S
n+
Floating Gate
Control Gate
V_G
p-
n+
V_D
Interpoly Oxide



1. Scaled. Two-micrometer design rules squeeze the E-PROM cell down to 6 by 6 μm. The active channel area, beneath the floating polysilicon gate, is just 1 by 1.2 μm. The n$^+$ regions are 0.6 μm deep.

by M. Van Buskirk, M. Holler, G. Kondi, B. Lee, S. Lee, D. Tang, G. Tong, S. Fouts, P. Dang, and W. Fisher, *Intel Corp., Santa Clara, Calif.*

256Kb CMOS EPROM

William Ip, Te-Long Chiu, Tsung-Ching Wu, Gust Perlegos

SEEQ Technology, Inc.

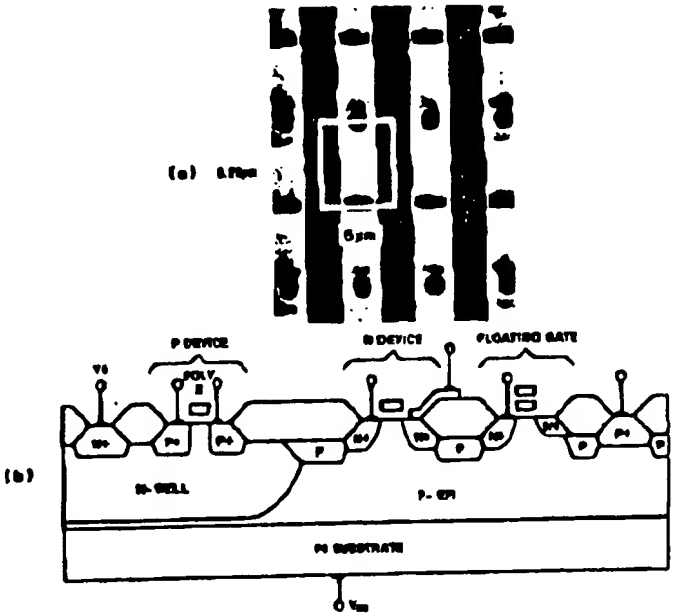


FIGURE 1—SEM photograph of 6μm x 6.25μm cell in array (a), cross sectional view of the CMOS EPROM technology (b).

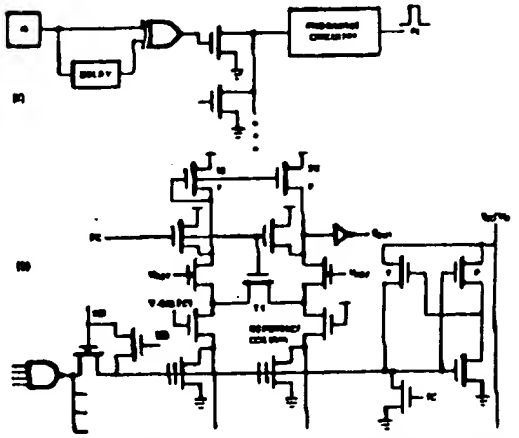


FIGURE 2 Address edge detection circuit (a), precharging and sense amplifier (b).

Physical Characteristics	
Minimum feature size	1.5μm
Cell size	6μm x 6.25μm
Die size	4.57mm x 4.57mm
Organization	32k x 8
Electrical Characteristics	
ICC (standby)	100μA
IPP (standby)	100μA
Active power	100mW at 5MHz
Access time	125ns (typ.)
Programming voltage	12 to 16V
Programming time	0.5ms/byte

TABLE 1—Characteristics of 256K CMOS EPROM

EPROM Deprogramming

History

- Recurrent problem with floating-gate EPROM devices

Impact on Devices

- Previously written memory bits become erased when exposed to high voltages on device control-gate with source and drain grounded or at low potential
- Failure mechanism is also manifested as immediate retention loss or failure to write (program)

- Also as Read-disturb

Impact on Product Yield

- Deprogramming reduces yield

EPROM Device Operational Modes

Operation \ Node Voltage		V_S	V_G	V_D
Read		Gnd	5 V	≈1.6 V
Selected Device	Write	Gnd	≈25 V	16–18 V
Unselected Device	Write Inhibit on Same Word Line	Gnd	≈25 V	Gnd
	Write Inhibit on Same Bit Line	Gnd	≈Gnd	16–18 V

EPROM Deprogramming

Deprogramming Model

- Loss of stored charges from floating-gate to control-gate on unselected devices during Write operation

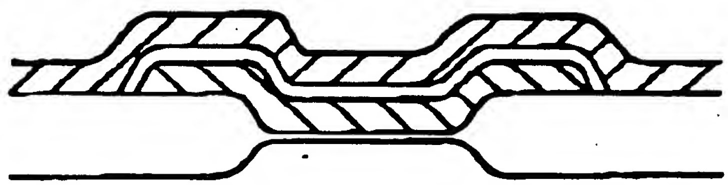
Loss Mechanism

- Asperities or other surface features found on floating-gate polysilicon surface or in the interpoly oxide cause localized enhancement of electric field which promotes Fowler-Nordheim emission of stored charges

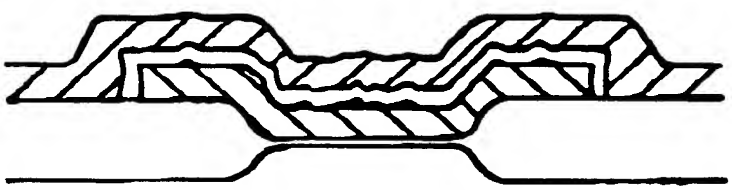
- Overly sharp edges on floating-gate poly under control-gate overlap region causing Fowler-Nordheim emission of stored charges

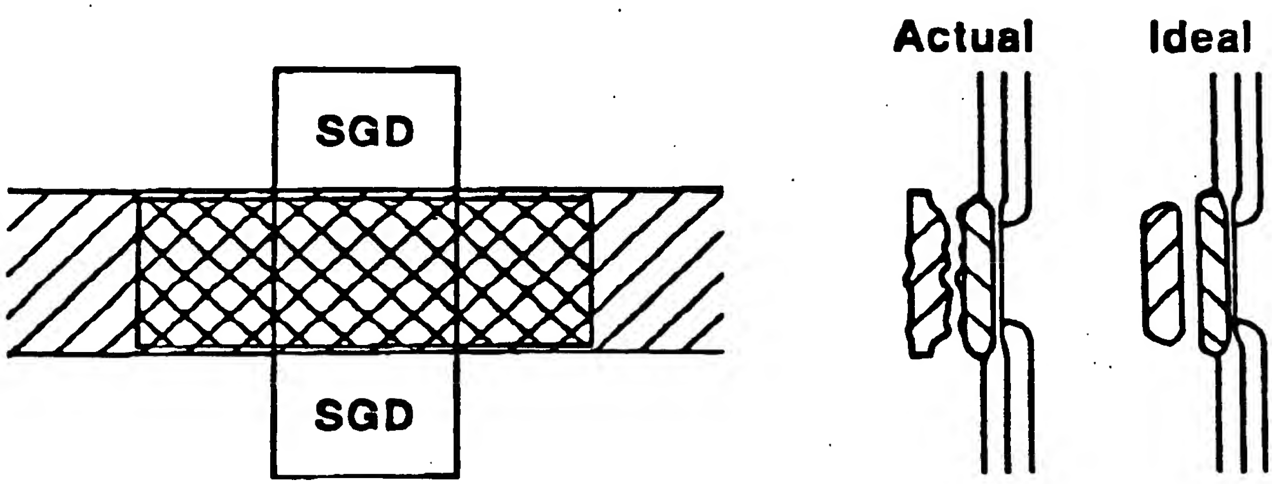
3808 EPROM Poly Profiles

Ideal



Actual





(Drawing courtesy of A. Mecchi)

1384-YHB

FAIRCHILD
A Schlumberger Company

The Impact of Procsing Conditions on EPROMsperities and Device Deogramming

Yukun Hsia anden Y. C. Mei

EPROM Deprogramming

Potential Processing Solutions

- **Asperity Related**
  - Poly deposition temperature
  - Poly doping temperature
  - *Increased poly doping level*
  - Poly anneal
  - Pre-oxidation clean
  - *Higher interpoly oxidation temperature*
  - HCl interpoly oxidation
  - Post-oxidation anneal
- **Edge Effect Related**
  - Etch slope control through alteration of etch ambient
  - Higher interpoly oxidation temperature

Experiment Result Summary

(Exclusive of interpoly oxide temperature and doping level)

Asperity Related

- Lower poly deposition temperature
  - Problem with uniformity control
- Increased poly doping temperature
  - Deprogramming increased
- Poly anneal
  - No effect discernible
- Pre-oxidation RCA clean
  - No effect discernible
- HCl interpoly oxidation
  - Small improvement observed
- Post-oxidation anneal
  - Not investigated

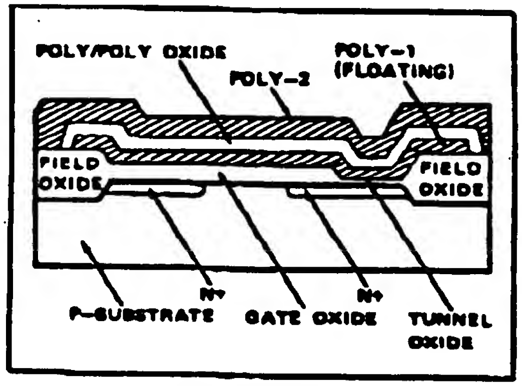
Edge related

- Etch slope control
  - SF_6 showed small improvement

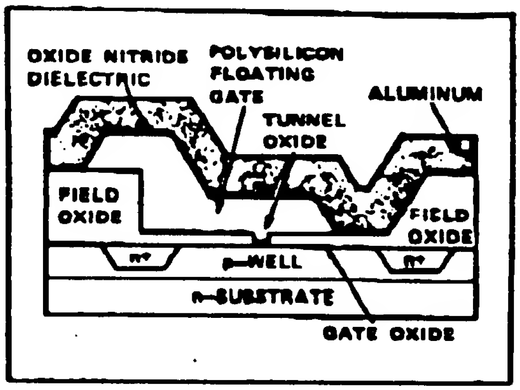
Summary of Successful Results on Deprogramming Experiments

Interpoly oxide temperature and doping level experiments

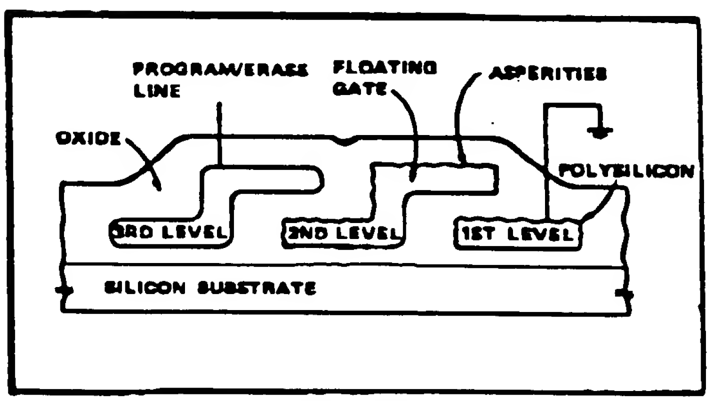
Process Variation	Total Wafers	Total	Good Func	Good Write	Good Ver 1	Good Ver 2	Good Die	% Yield	512 Bits Sampled	Bits	% Depro
IPOX	5 2(2030) 3(2031)	1014	588 58%	269 46%	249 93%	228 92%	216 95%	21	497	7	0.003
V/I	5 5(2030)	940	468 50%	325 69%	318 98%	317 99%	317 100%	34	379	0	0.000
Control	5 4(2030) 1(2035)	949	471 50%	325 69%	217 67%	88 41%	36 41%	4	366	181	0.097



INTEL EEPROM



HUGHES EEPROM



XICOR EEPROM

Cross-Sections of Floating Gate EEPROMs

A 55ns CMOS EEPROM

Richard Zaman, Chun Ho, Thomas Cheng

Exel Microelectronics, Inc.

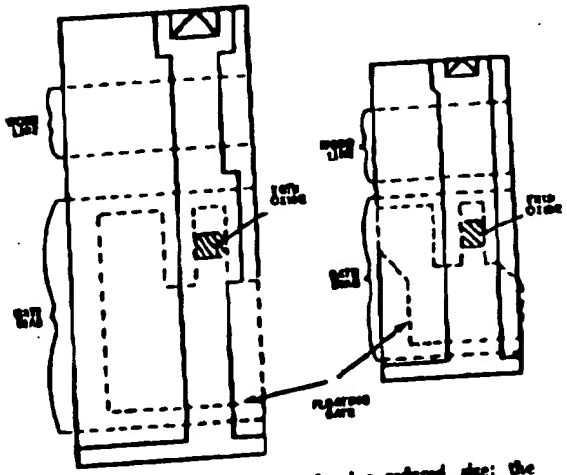


FIGURE 1–Cell comparison showing reduced size; the 16K EEPROM cell uses 2µm design rules; scaled EEPROM cell uses 1.5µm design rules.

FABRICATION	
TECHNOLOGY	CMOS FLOATING GATE
DESIGN RULES	1.5µm
LITHOGRAPHY	STEPPER
PHYSICAL CHARACTERISTICS	
DIE SIZE	141 x 278 mils
ORGANIZATION	4K x 8
PACKAGE	24 PIN
DC PERFORMANCE	
OPERATION	FULLY STATIC
SUPPLY VOLTAGE	5 VOLTS
ACTIVE CURRENT	50mA
STANDBY CURRENT	10µA (CMOS INPUT LEVELS)
I/O LEVELS	TTL
AC PERFORMANCE	
ADDRESS ACCESS TIME	55 ns
CHIP SELECT TIME	40 ns
WRITE TIME	1 ms

TABLE 1–Summary performance.

TRANSISTOR TYPE*	OPERATING VOLTAGE (V)	JUNCTION DEPTH (µm)	OXIDE THICKNESS (Å)	CHANNEL LENGTH (µm)
HIGH VOLTAGE	21	0.8	650	3.5
LOW VOLTAGE	5	0.3	300	1.5

*FOR BOTH N AND P CHANNEL

TABLE 2–Junction depth, oxide thickness and channel length for N- and P-channel high and low-voltage transistors used in chip.

A 64Kb CMOS EEROM with On-Chip ECC

Sanjay Mehrotra, Tsung-Ching Wu, Te-Long Chiu, Gust Perlegos

SEEQ Technology, Inc.

Process	N-well CMOS on epi
Minimum feature size	1.5μm
Metal pitch	6μm
N⁺ to P⁺ spacing	9μm
Poly-Si I Gate Oxide	400Å
Poly-Si II Gate Oxide-Nitride	400Å
Tunnel dielectric	85Å Oxynitride
Cell size	85 sq. μm
Die size	182 sq. mils
Programming time	1ms
Endurance	$>10^6$ program/erase cycles
Access time	100ns
Active current	20mA
Standby current	1μA

TABLE I –Characteristics of 64Kb CMOS EEROM

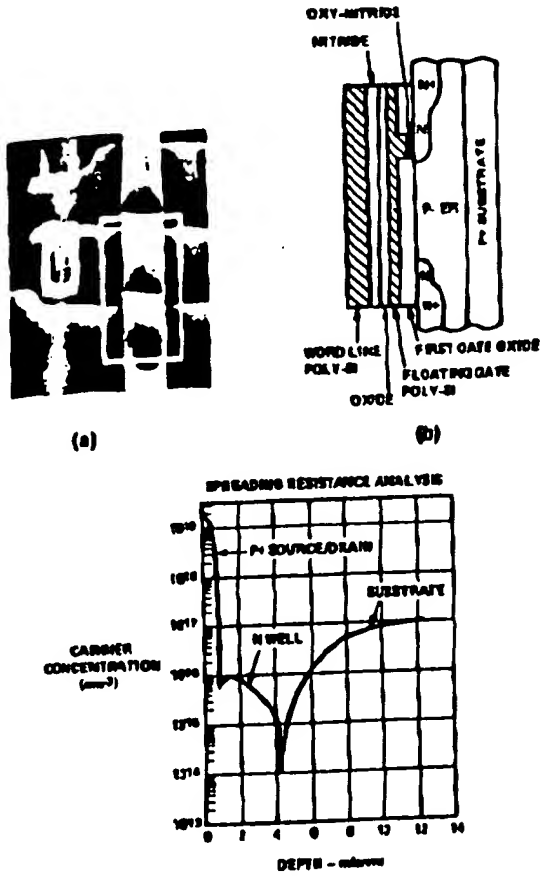


FIGURE 1–(a)–SEM photograph of a two-transistor EEROM cell with byte selection device, (b)–cross sectional view of floating poly EEROM, (c)–spreading resistance measurements under P⁺ source/drain diffusion.

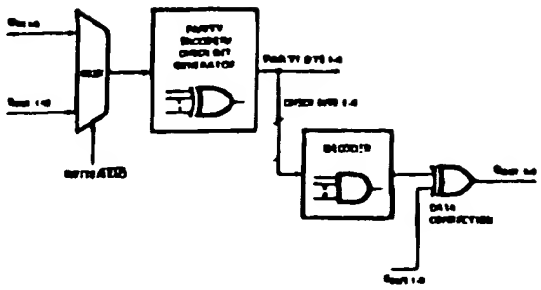


FIGURE 2–Functional block diagram of on-chip error checking and correcting circuits.

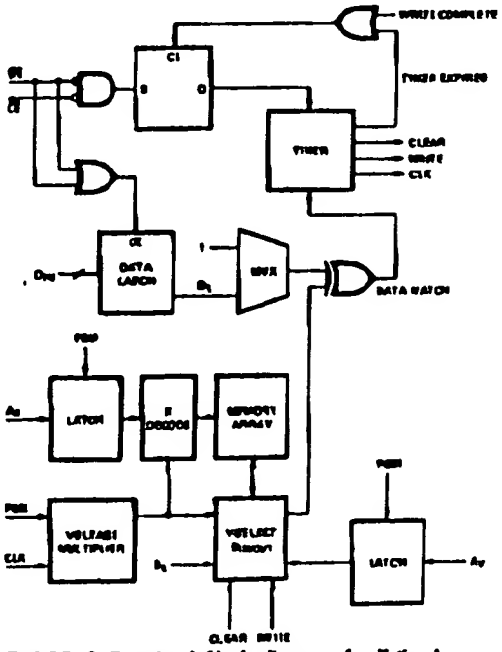


FIGURE 3–Functional block diagram of self-timed programming operation.

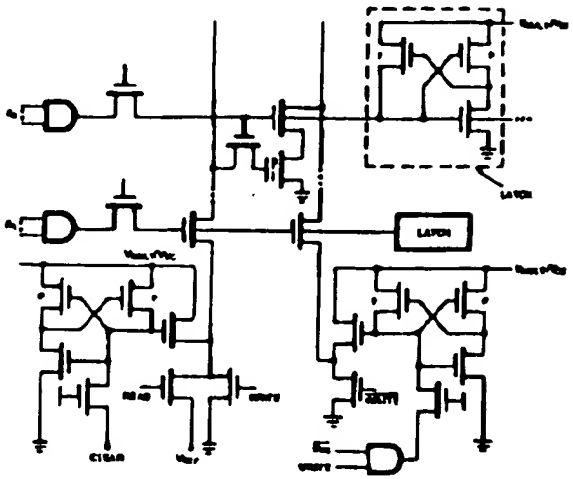


FIGURE 4–High voltage decoding during programming.

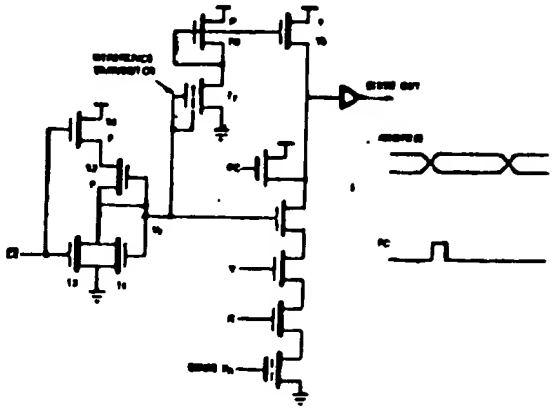


FIGURE 5–Schematic of sense amplifier.

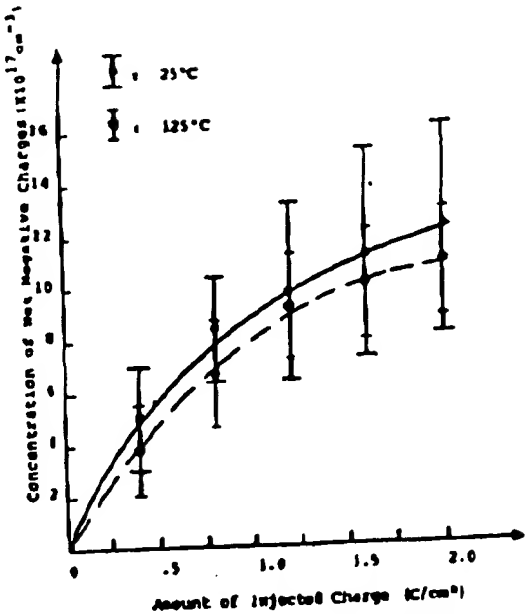


Fig. 1. Effect of Temperature on Charge Trapping in Oxynitride

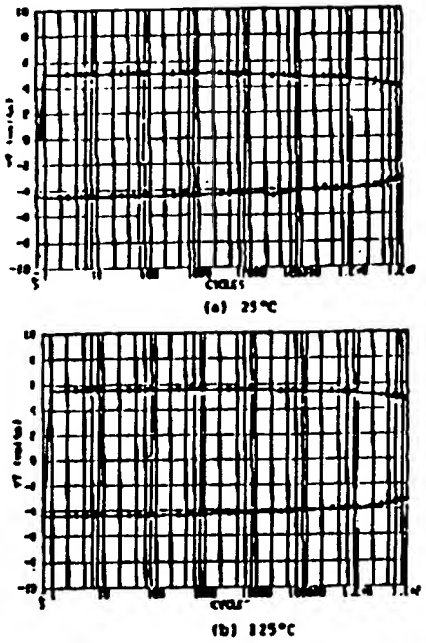


Fig. 2. Effect of Temperature on the Endurance of Single EEROM Cells. Plotted are W/E Threshold Window vs. Number of W/E Cycles.

EEDM 89

HIGH TEMPERATURE AND EXTENDED ENDURANCE CHARACTERISTICS OF EEROM

Ching S. Jenq, Ping Wong and Bharati Joshi
SEEQ Technology, Inc, San Jose, Ca
and
Chenming Hu
University of California, Berkeley, Ca

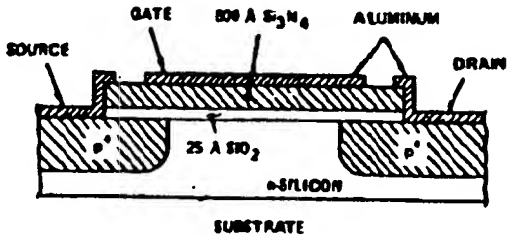


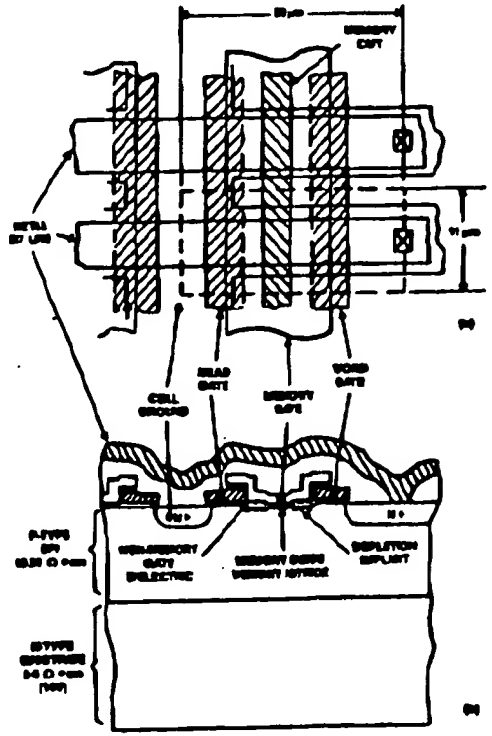
Fig 1
MNOS Transistor

+5V-Only 32K EEPROM

Darrel D. Donaldson, Edward H. Hannigford, Louh J. Toth

NCR Microelectronics Division

FIGURE 1—The 3-gate memory cell, layout (a), cross section(b).



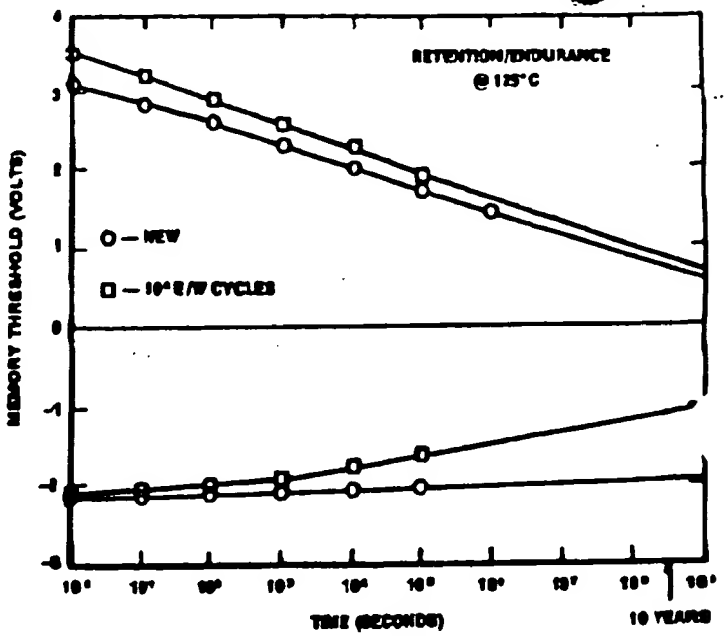


FIGURE 2—Typical data retention/endurance curves measured on a 4Kb test chip. Data points are determined by checking for a read failure while varying the memory gate voltage.

PROCESS	SNOS (SILICON-NITRIDE-OXIDE-SILICON)
OPERATION	FULLY STATIC
ORGANIZATION	4K WORDS X 8 BITS
PAGE SIZE	16 WORDS
PACKAGE	28 PIN
CELL SIZE	.39 mil²
CHIP SIZE	42K mil² (27mm²)
ERASE MODES	BULK (4K BYTES) PAGE (16 BYTES)
WRITE MODES	1 TO 16 BYTES
ERASE/WRITE TIME	100 ms/10 ms
ENDURANCE	10^4 ERASE/WRITE CYCLES
RETENTION	10 YEARS @125°C
READ CYCLES	UNLIMITED
ACCCESS TIME	300 n s
ACTIVE POWER	450 mW
STANDBY	150 mW
TEMPERATURE RANGE	-55 TO 125°C

TABLE I—Main features of the 32K EEPROM.

A 5V-Only EEPROM with Internal Program/Erase Control

Art Lancaster, Bob Johnstone, Jeff Christ, Gerry Talbot, David Weston

Inmos Corp.

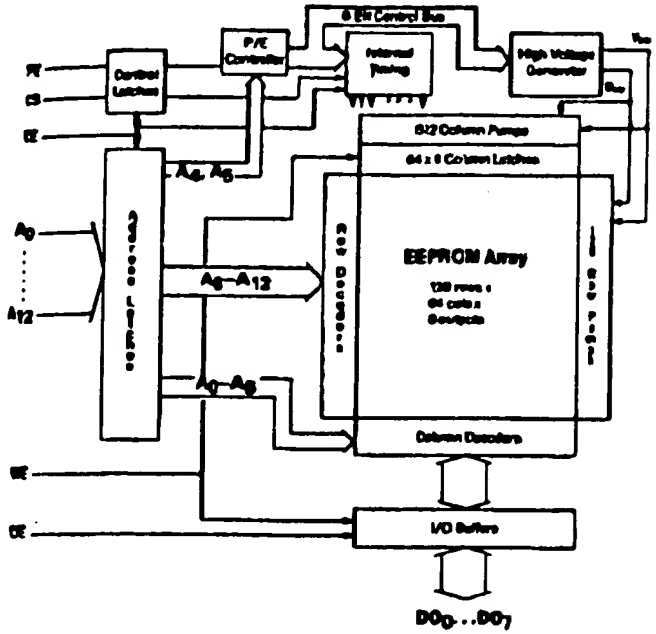


FIGURE 2—Functional block diagram.

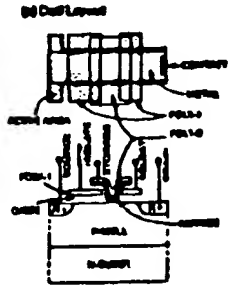
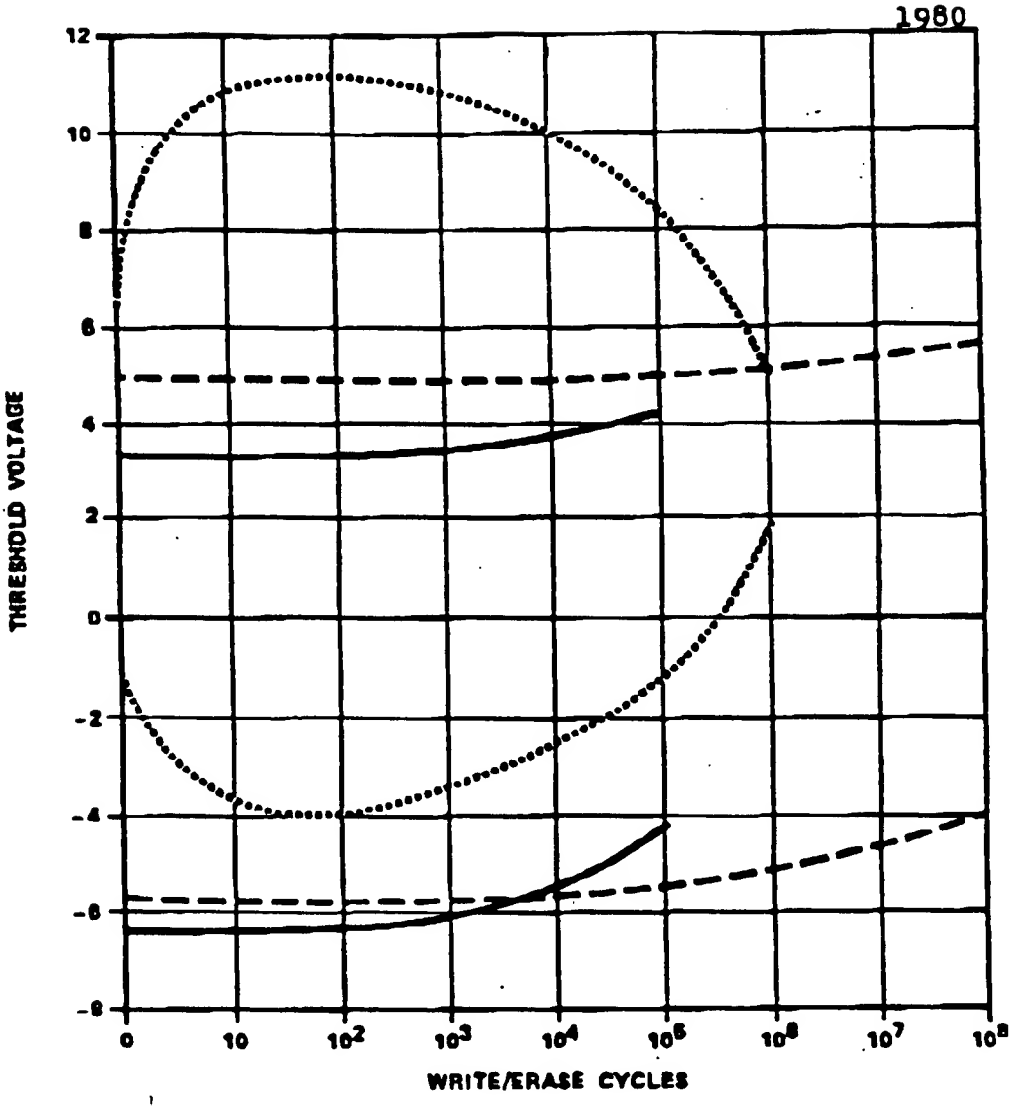


FIGURE 1—Mitsubishi memory cell.

(a) PROGRAM/ERASE MODE CONTROL			(b) SPECIFICATIONS		
A6 & A5 control during PE bit late Cycle				MIN	MAX
MODE	A6	A4	Read access time	<200 ns	–
Full-Array Erase	0	0	Cycle time	<380 ns	Unlimited
Row-Erase	0	1	Program time	10 ms	–
Latch-Latches-Row-Erase	1	0	Erase time (Row or Array)	100 ms	–
Program	1	1	Icc active	–	150 mA
			Icc standby	–	90 mA

FIGURE 3—Program/erase control and specifications.



LEGEND:

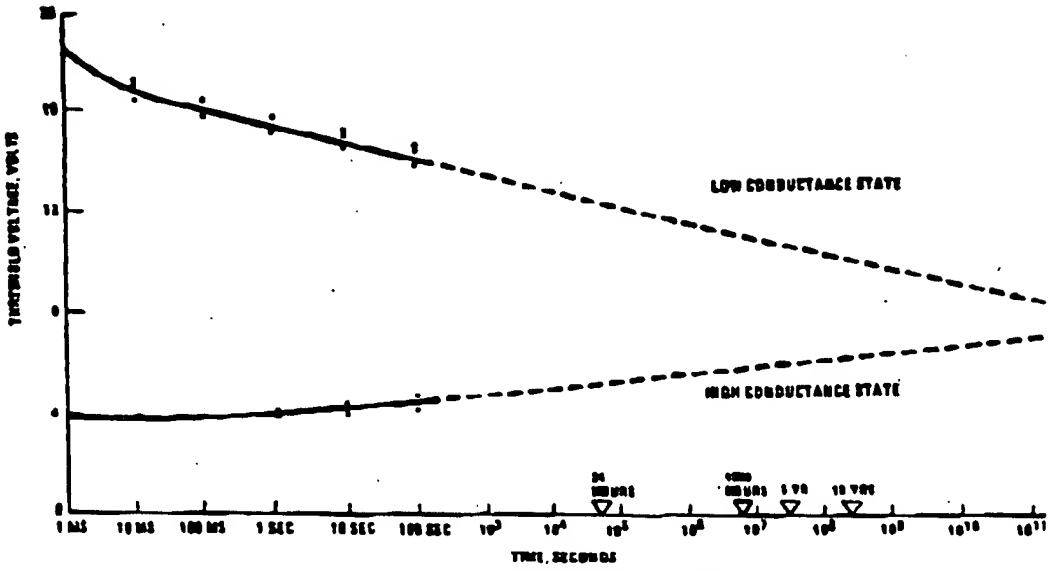
INTEL "FLOTOX"
W - 10mS @ 20V
E - 10mS @ 20V

HITACHI MNOS
W - 1mS @ 25V
E - 1mS @ 25V

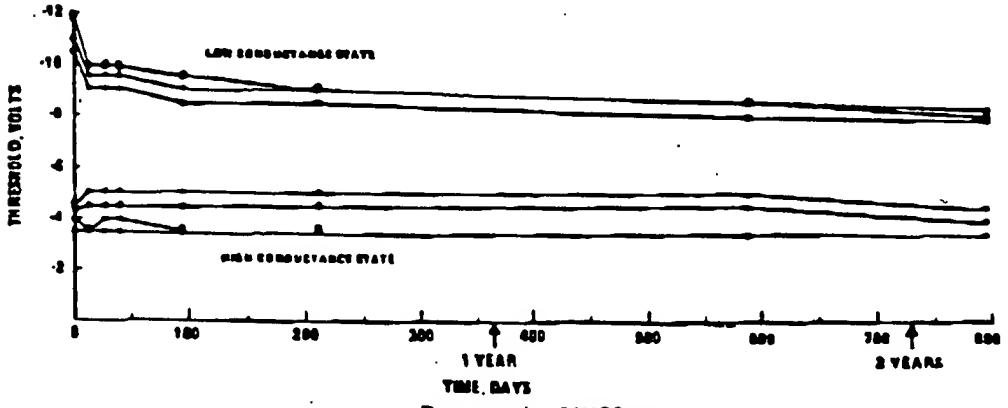
MCDONNELL DOUGLAS MNOS
W - 200μS @ 22V
E - 1mS @ 22V

Figure Comparison of the Effect of Endurance Cycling on Memory Thresholds for the MDC MNOS, Hitachi MNOS and Intel Flotox Nonvolatile Memory Transistors

MNOS Data Retention



Zero-bias retention plot of the MNOS.

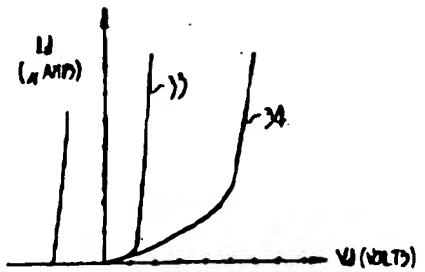


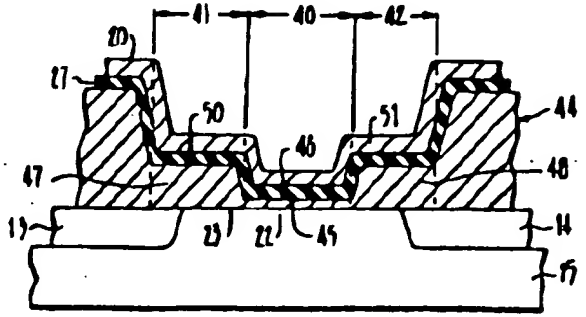
Data retention, MNOS array.

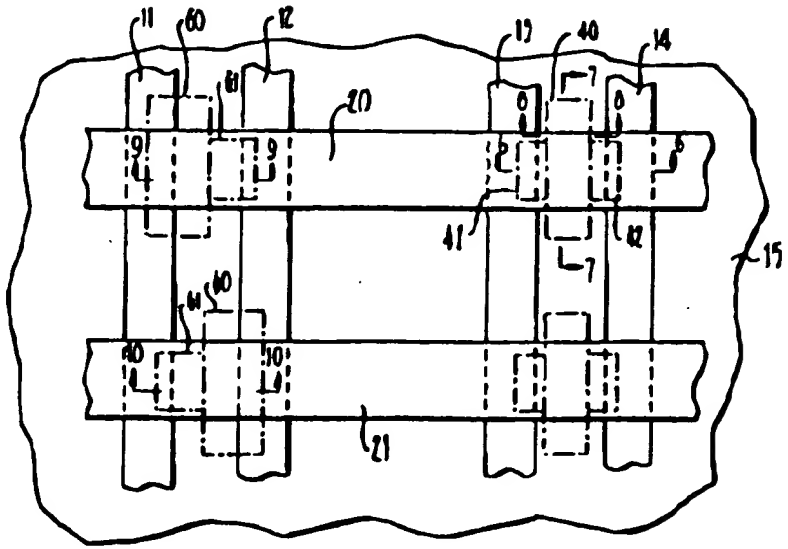
MEIA: MNOS LSI MEMORY DEVICE

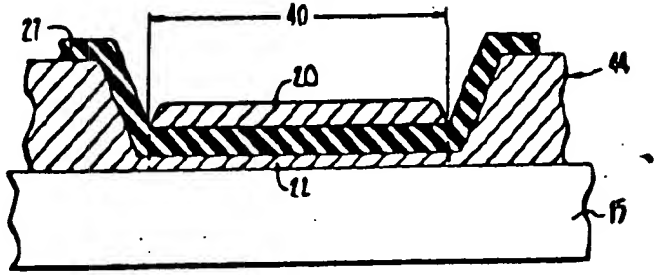
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-24, NO. 5, MAY 1977

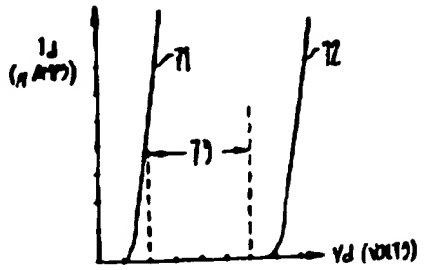
MNOS MEMORY DEVICE











United States Patent 4,063,267

Inventor: Yukun Hsia, Saratoga, Calif. Dec. 13, 1977

YUKUN HSIA

K. L. NGAI

MNOS TRAPS AND TAILORED TRAP DISTRIBUTION GATE DIELECTRIC MNOS

PRESENTED AT THE 1979 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES

AUGUST 27-29, 1979, TOKYO, JAPAN

MICROSCOPIC MODEL OF MEMORY TRAPS

CHEMICAL REACTION FOR FILM FORMATION

$$3\,Si\,H_4 + 4\,NH_3 \longrightarrow Si_3N_4 + 12\,H_2$$

SATURATED Si–N BOND

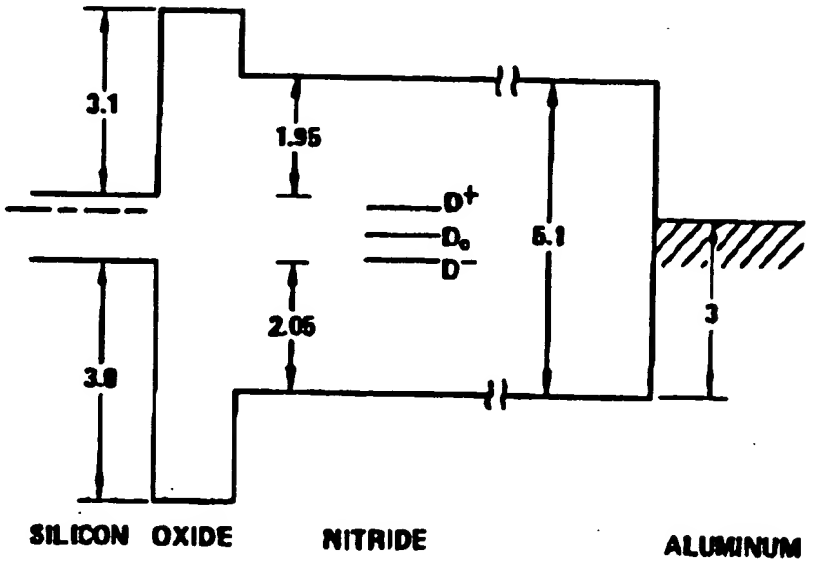
DANGLING Si–BOND

ELECTRON EXCHANGE TO FORM AMPHOTERIC TRAPS

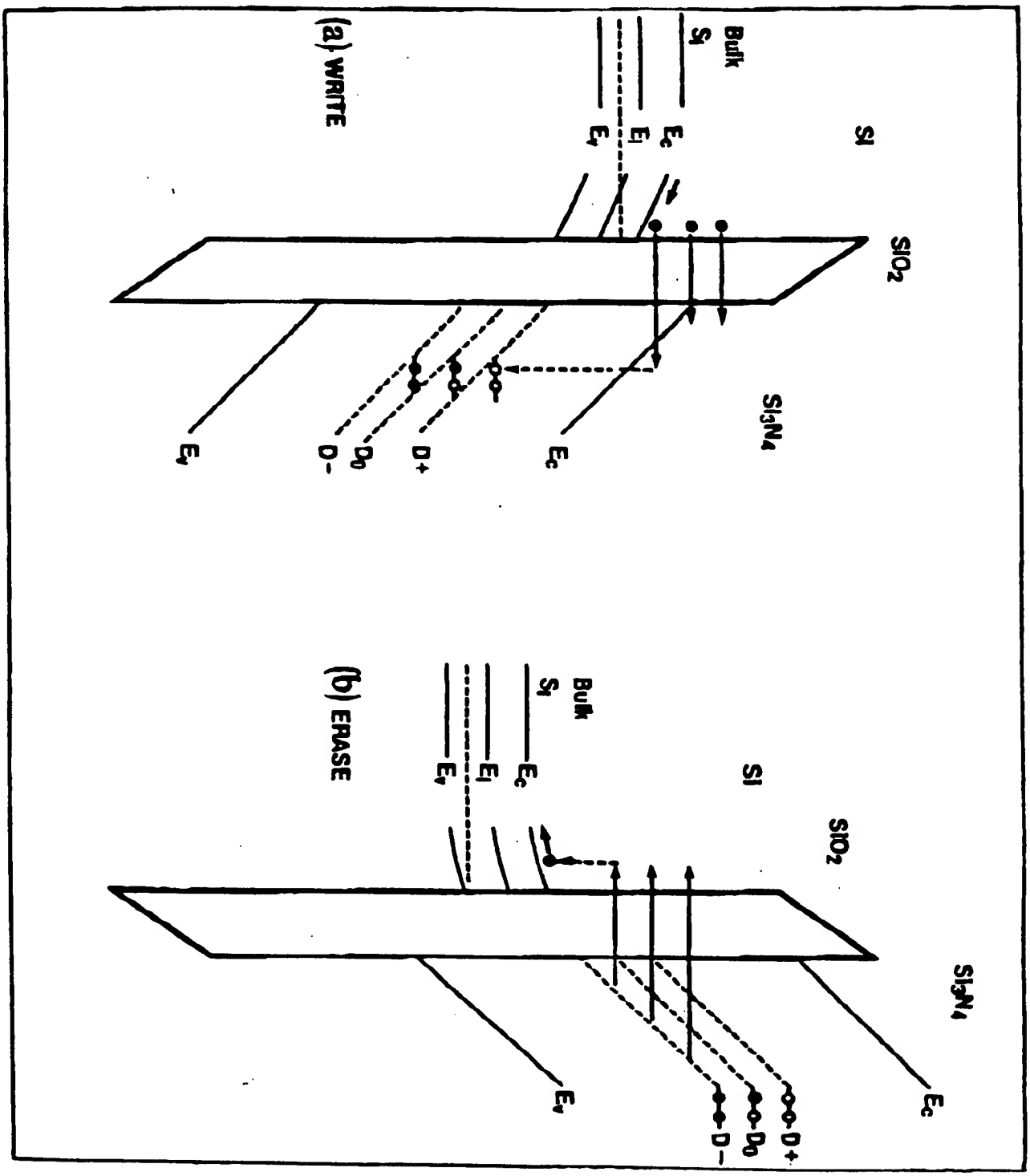
$$2\,N_3Si\cdot \longrightarrow N_3Si: + N_3Si$$

$$2\,D^0 \longrightarrow D^+ \text{ TRAP} + D^- \text{ TRAP}$$

ELECTRON ENERGY DIAGRAM OF MNOS STRUCTURE



ALL ENERGY VALUES IN EV


(a) WRITE
Bulk
Si
Si
SiO_2
Si_3N_4
E_v
E_i
E_c
D^-
D_0
D^+
(b) ERASE
Bulk
Si
Si
SiO_2
Si_3N_4
E_v
E_i
E_c
D^-
D_0
D^+

PROPERTIES OF NITRIDE APTLY INTERPRETED BY THE MODEL

- ELECTRON AND HOLE TRAPS ARE EQUAL IN NUMBER
- CHARGE TRAPS ARE DISTRIBUTED IN THE NITRIDE BULK
- TRAPS ARE CHARGED
- EXCESS SILICON IN NITRIDE IS OBSERVED WITH SPECTROSCOPY
- LOWER NH_3/SIH_4 RESULTS IN LARGER THRESHOLD WINDOW
- N IMPLANT INCREASES NET POSITIVE FIX CHARGES WITH NEGATIVE SHIFT OF C-V HYSTERESIS
- B IMPLANT INCREASES NET NEGATIVE FIX CHARGES WITH POSITIVE SHIFT OF C-V HYSTERESIS

EFFECT OF HYDROGEN ON MEMORY TRAPS

- $\equiv Si-H$ BONDS ARE OBSERVED IN LOW TEMPERATURE DEPOSITED NITRIDE
- $2\equiv Si-H \longrightarrow 2\equiv Si- + H_2$
- SIMILARLY, DURING ENDURANCE CYCLING, IT IS POSTULATED THAT

$$\equiv Si-H + h^+ \longrightarrow \equiv Si- + H^+$$

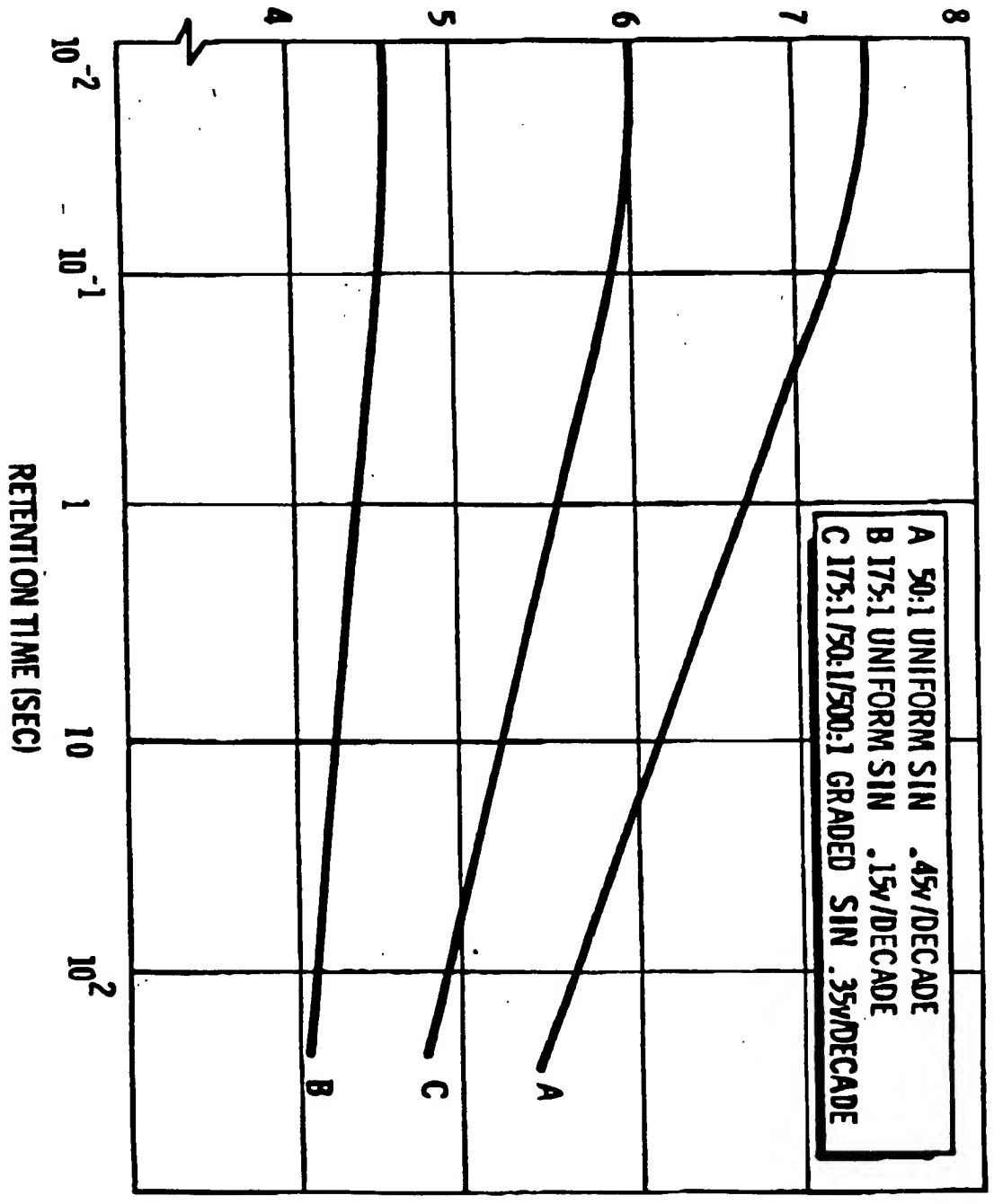
AND/OR

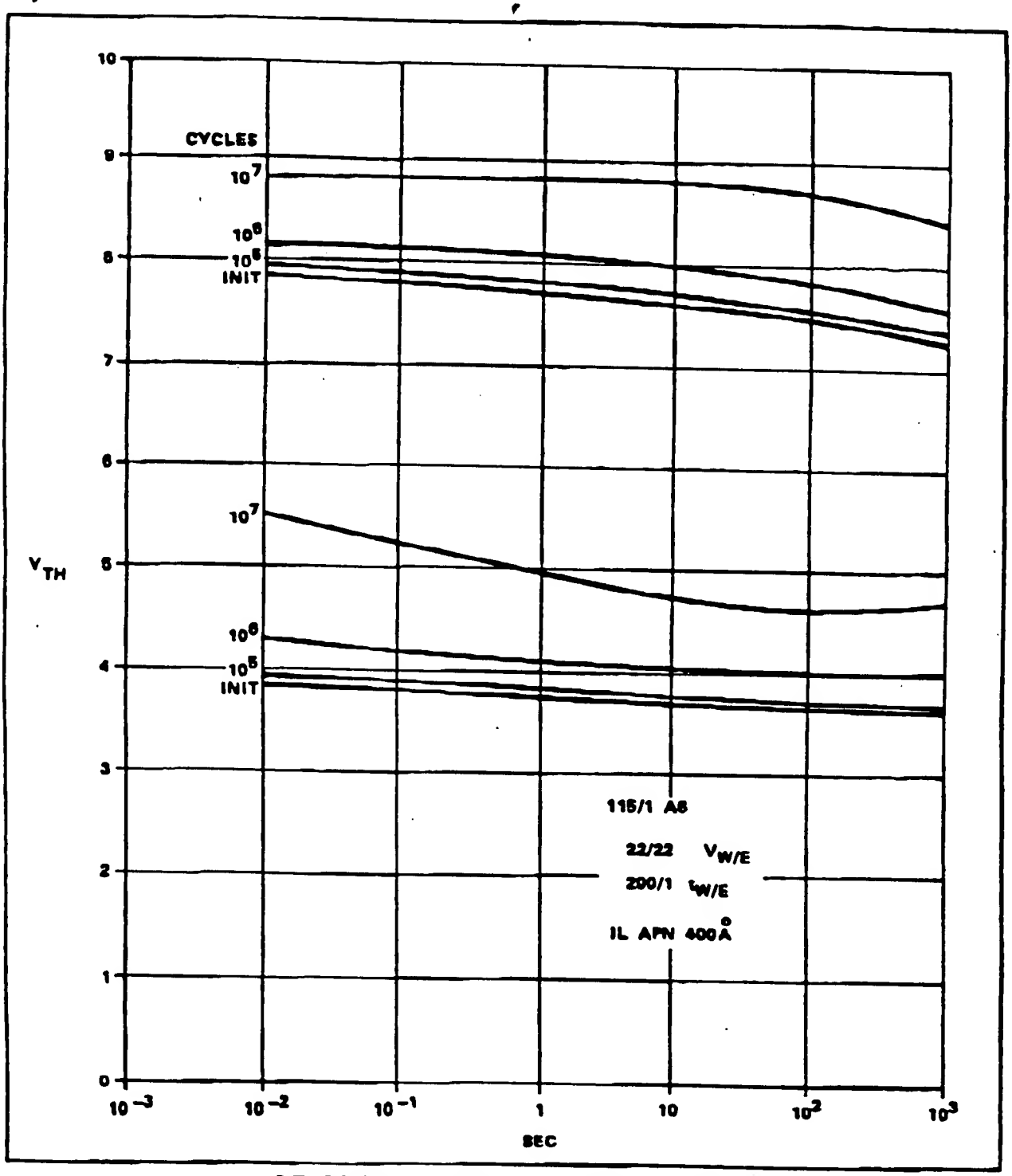
$$\equiv Si-H + h^+ + \equiv Si-\underset{\underset{\text{III}}{Si}}{N}-Si \longrightarrow \equiv Si- + \equiv Si-\underset{\underset{\text{III}}{Si}}{N}-H + \equiv Si^+$$

MNOS THRESHOLD WINDOW (ΔV_T) VERSUS NH_3:SiH_4 RATIO USED IN NITRIDE DEPOSITION (770°C NITROGEN CARRIER CVD NITRIDE)

NH_3:SiH_4 RATIO	250:1	175:1	125:1	75:1	50:1
V_T IN VOLTS	9.9	10.8	11.7	14.4	15.7

MNOS RETENTION VS SIN COMPOSITION

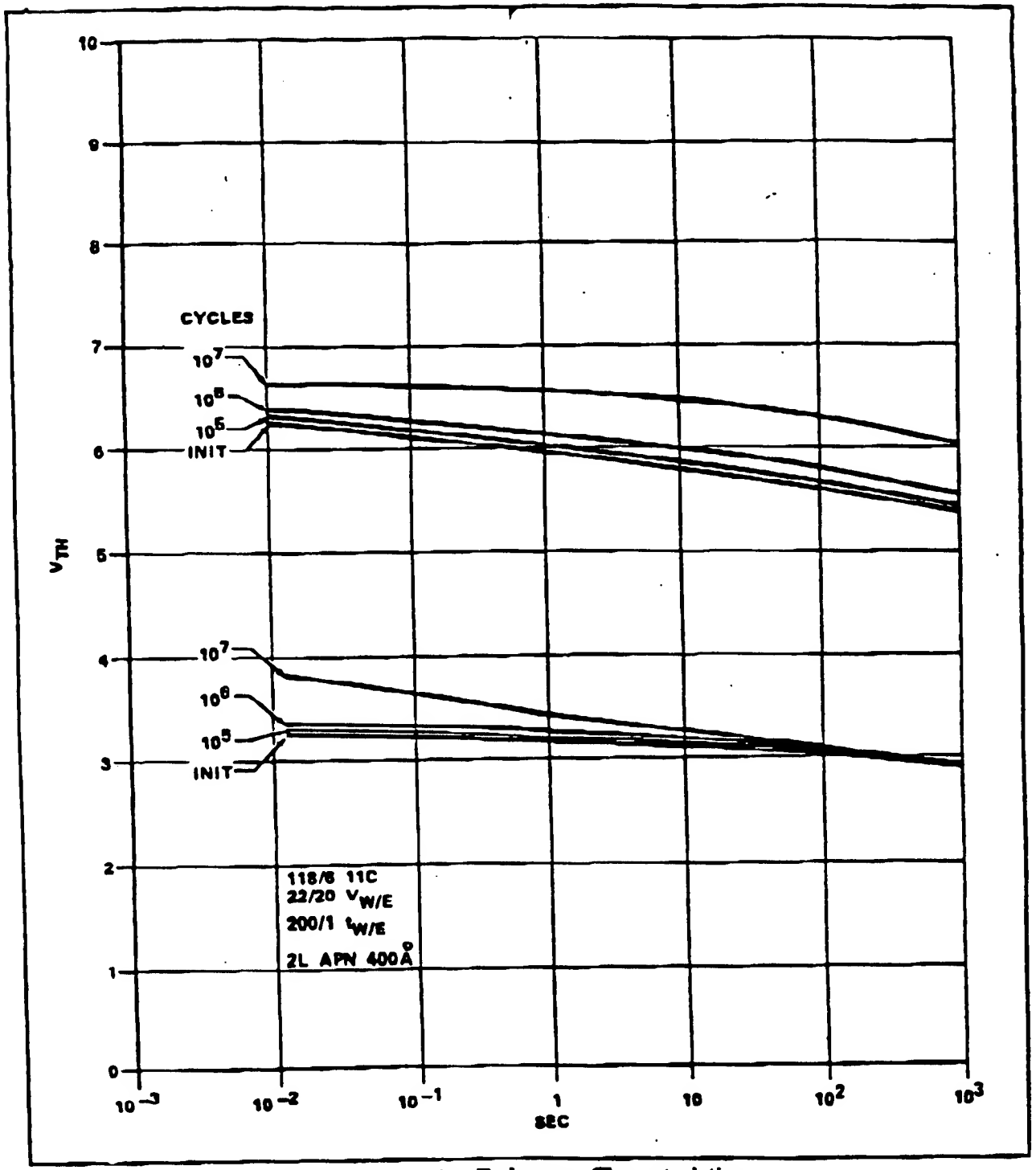




MNOS Retention-Endurance Characteristics

Yukun HSIA, Eden MEI and Kia L. NOAI

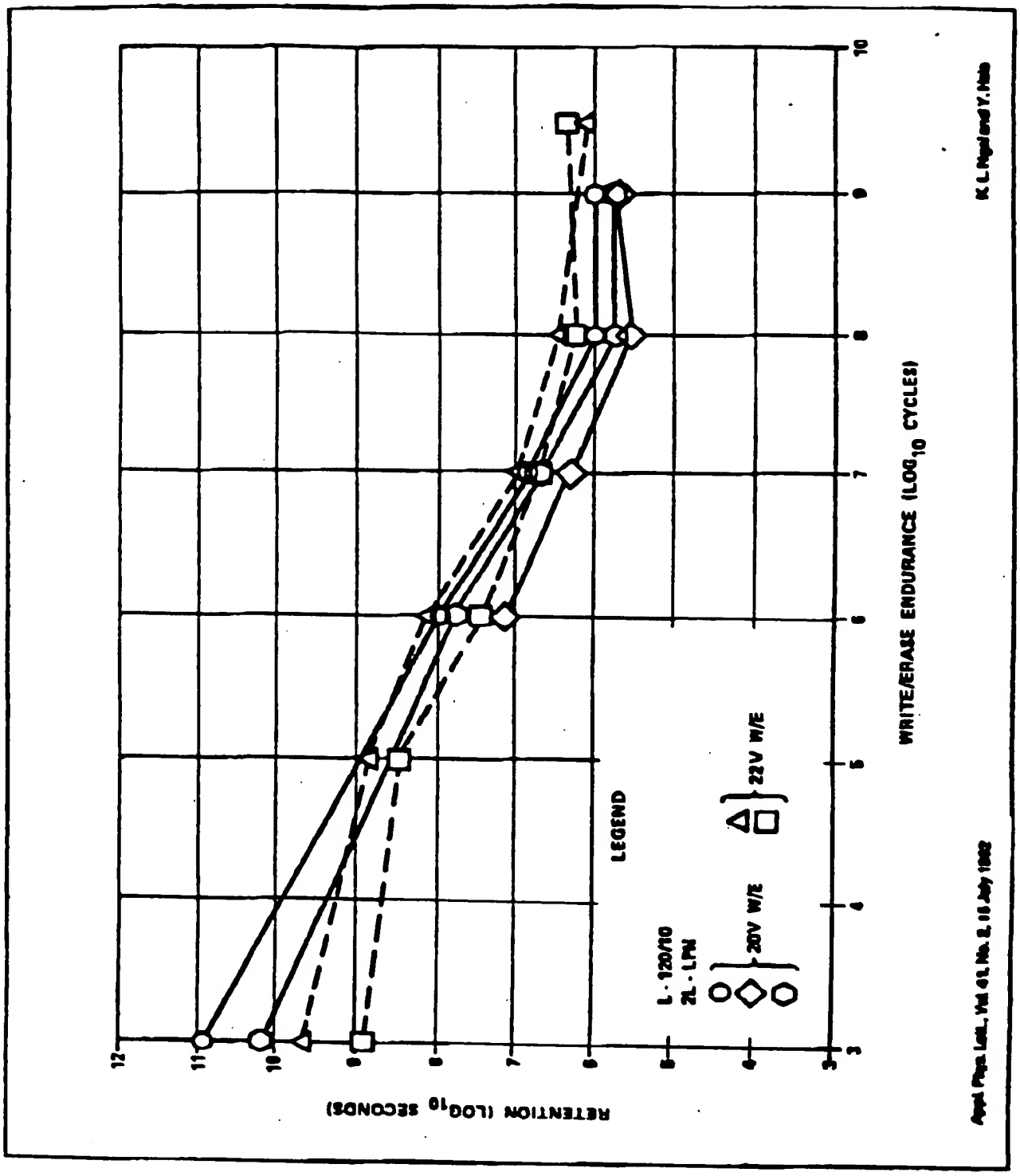
Proceedings of the 14th Conference (1982 International) on Solid State Devices, Tokyo, 1982;
Japanese Journal of Applied Physics, Volume 22 (1983) Supplement 22-1, pp. 89-93

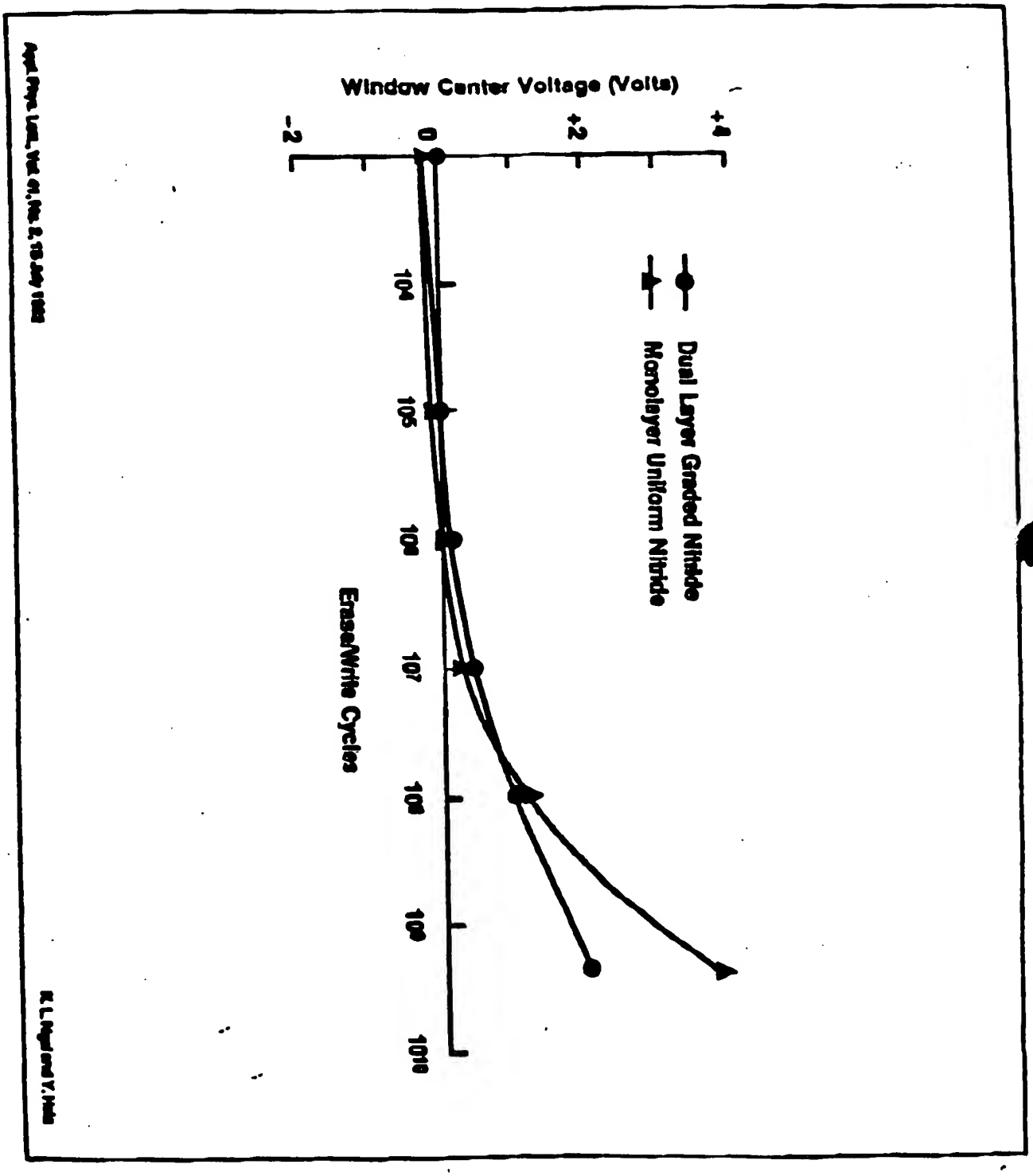


MNOS Retention-Endurance Characteristics
Graded Nitride Dielectric

Yukun Hsia, Eden Mei and Kia L. Ngai

Proceedings of the 14th Conference (1982 International) on Solid State Devices, Tokyo, 1982;
Japanese Journal of Applied Physics, Volume 22 (1983) Supplement 22-1, pp. 89-93


WRITE/ERASE ENDURANCE (LOG_{10} CYCLES)
RETENTION (LOG_{10} SECONDS)
LEGEND
L-120/10
2L-LPN
20V W/E
22V W/E
12
11
10
9
8
7
6
5
4
3


Window Center Voltage (Volts)
-2
0
+2
+4
10⁴
10⁵
10⁶
10⁷
10⁸
10⁹
10¹⁰
Erase/Write Cycles
Dual Layer Graded Nitride
Monolayer Uniform Nitride

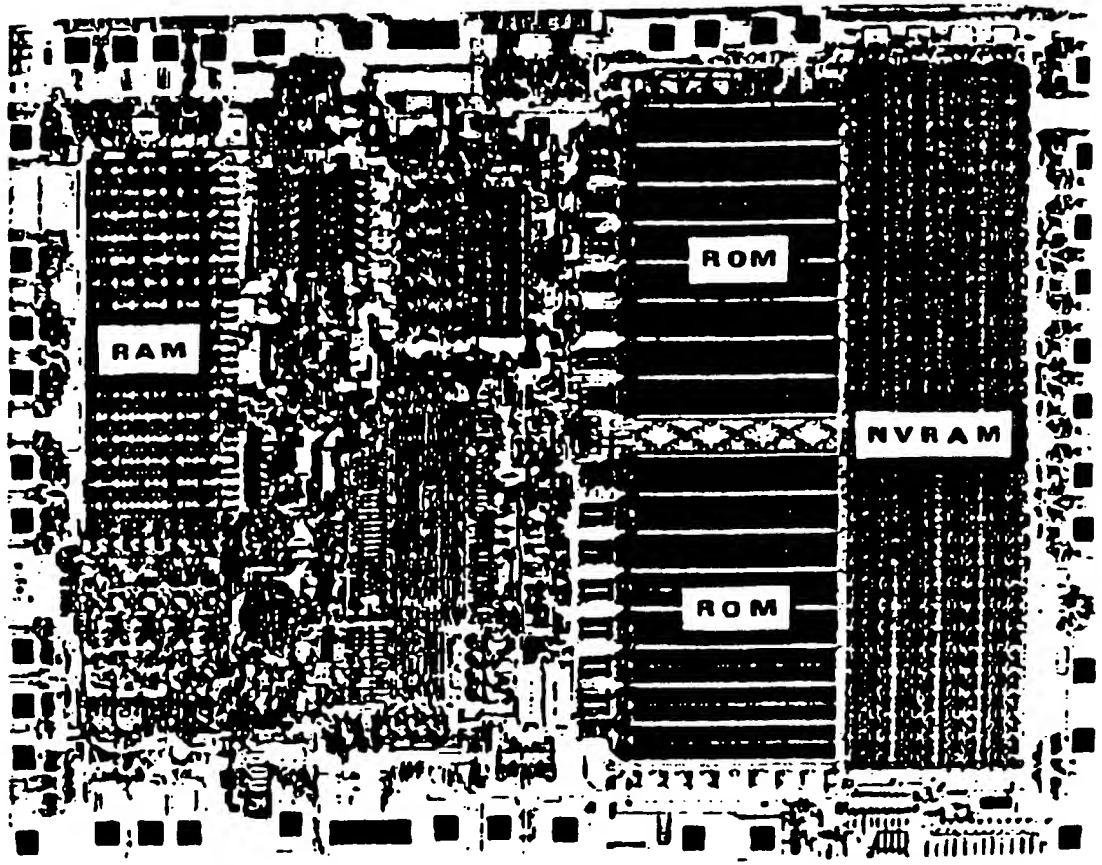
A 5V-Only Single Chip Microcomputer with Nonvolatile SRAM

Paolo Rolini, Roberto Finzinti, Maurizio Gaibotti

SGS-ATES, Milan, Italy

CELL CHARACTERISTICS	
PHYSICAL CHARACTERISTICS	
ELECTRICAL CHARACTERISTICS	

TABLE I—Physical, electrical and performance characteristics



Photograph of 5V-only single chip microcomputer with nonvolatile static RAM.